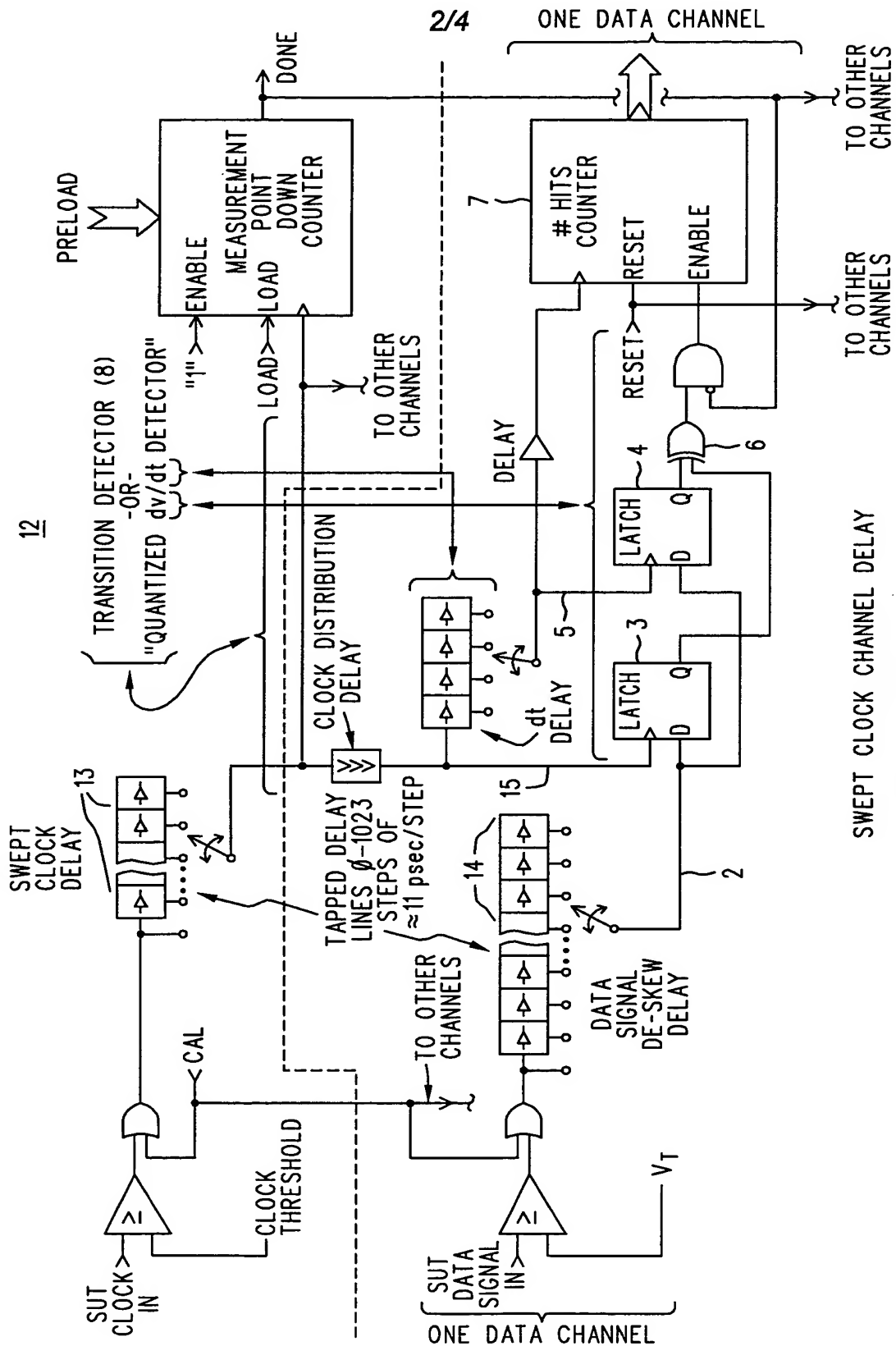


SWEPT DATA CHANNEL DELAY

FIG. 1 (PRIOR ART)



SWEPT CLOCK CHANNEL DELAY

FIG. 2 (PRIOR ART)

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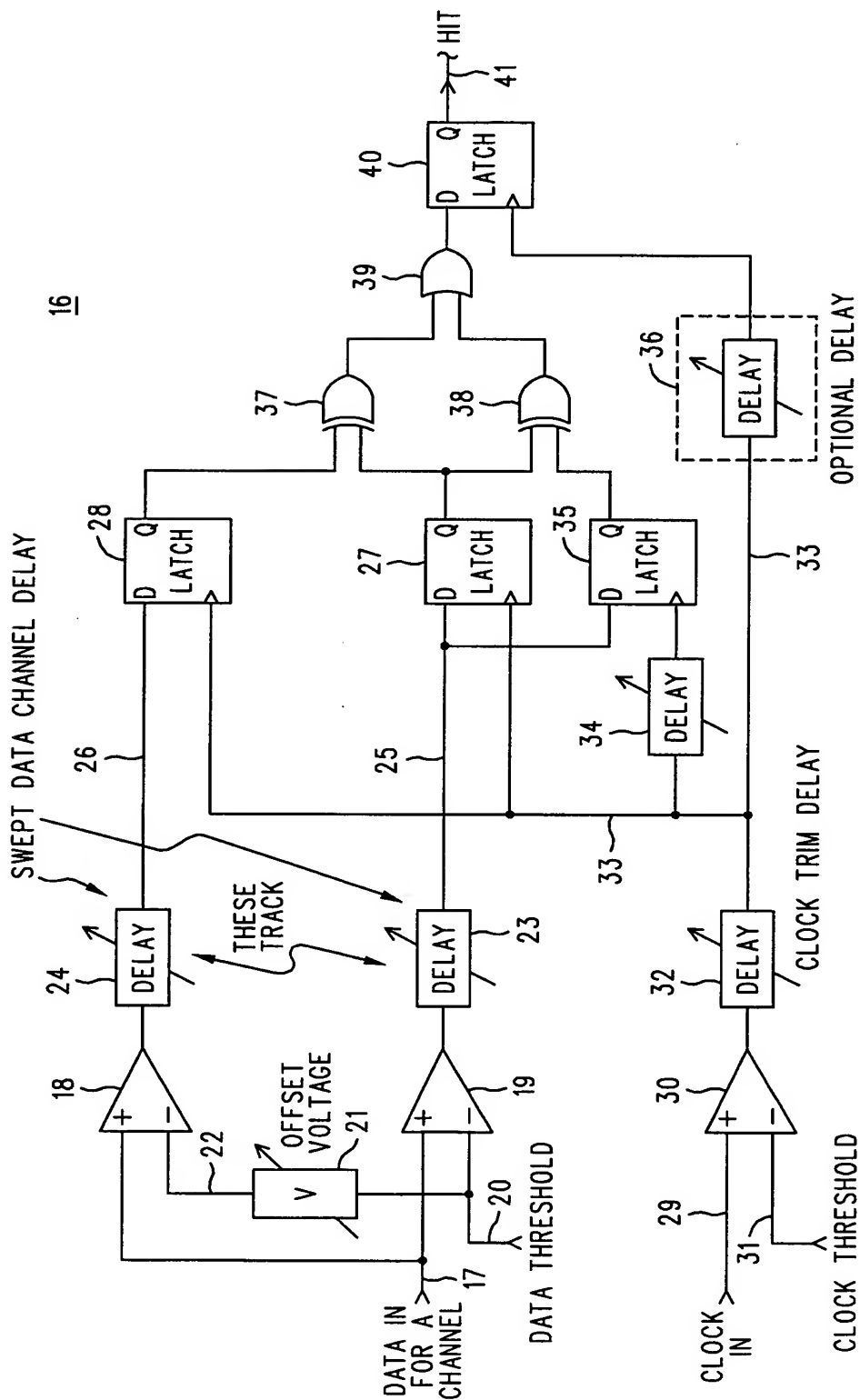


FIG. 3

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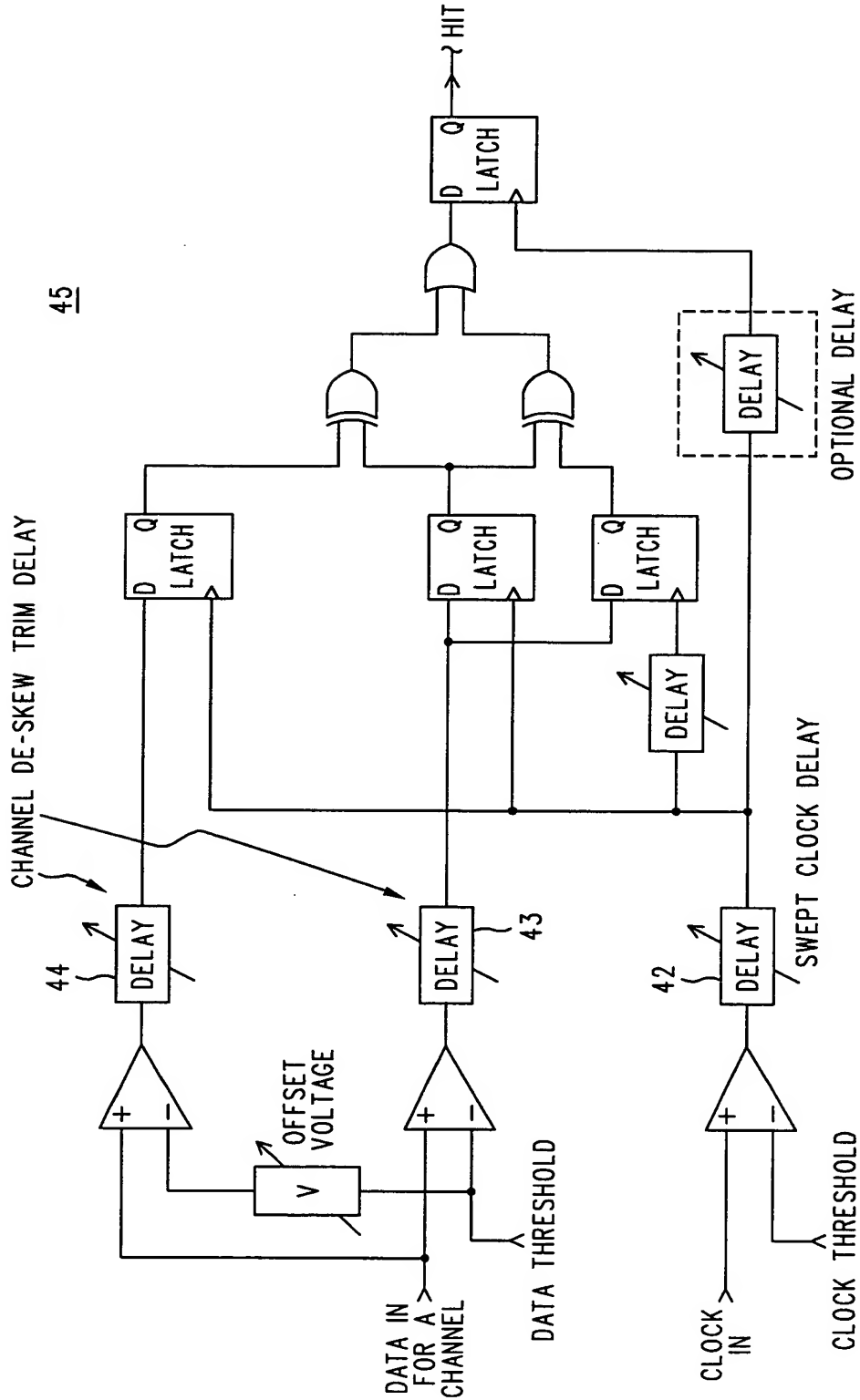


FIG. 4